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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,382	12/05/2001	Louise A. Koss	10010863-1	2960

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2133	3

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/008,382	Applicant(s) KOSS ET AL.	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *1-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 are presented for examination.

Drawings

2. The drawings are objected to because the functional blocks in FIG. 4 require appropriate legends describing the particular function without referring back to the specification. Suitable descriptive legends may be used subject to approval by the Office, or may be required by the examiner where necessary for understanding of the drawing. They should contain as few words as possible.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because the abstract of the disclosure does not comply with proper language and format. The abstract should be in narrative form and should avoid using legal phraseology often used in patent claims.

The expression "circuitry is disclosed which provides" should be changed to "circuitry provides".

The term "means" should be changed to the specific device related to the associate function.

The expression "circuits disclosed" should be changed to "circuits".

Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 1-7 are objected to because they require indentation. Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(m).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the following limitations: "each input/output circuit" in line 11, "of the self-test data comparisons" in line 18, and "of the self-test" in line 1. There is insufficient antecedent basis for these limitations in the claim.

Claims 2-8 are also objected because they depend upon a main objected claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhavsar et al. (US 6408401).

Regarding Claim 1, Bhavsar discloses an electronic circuit, such as a test and repair logic circuit (201) embedded in a RAM circuit chip 12 for performing a self-test on a random access memory array RAM cache 80 having a plurality of memory storage cells organized into a plurality of slice arrays (91), Column Slices (0-82) in the RAM array 81, as shown in FIGS. 1, 2 and 4, comprising:

A control circuit, such as RAM Test Algorithm Engine (207) of test and repair logic circuit (201), which generates address, data and read/write control signal (221) sequence.

An address selection circuit (Address and Read/Write Data path Logic 255), directed by the RAM Test Algorithm Engine (207) via the memory bus 20 to index through memory address 94 of RAM array 81.

An input/output circuit, such as a typical line driver/receiver I/O circuitry in the bi-directional memory bus (20, FIG. 1) for writing and reading data associated with each slice array (91).

The RAM Test Algorithm Engine 207 performs the self-test on the selected segment by alternately writing and reading 0s and 1s to the memory cells within the RAM segment 81 into its associated slice array (91) at an indexed memory address, according to a memory test algorithm. In the read operation, each data output bit 97 from the multiplexers 96 passes through the Column Repair Register and Logic 302, which are then compared by XOR gates 98 with expected reference data fed to D0 - D82 respectively. If the output value 97 is not the same as the expected written value D0 -D82, an XOR gate outputs a logic "1".

An error detection circuit, such as a column ID encoder circuit 100, collects comparison results from XOR 98 and upon an error, asserts an error signal 223 and provides the address 225 of a detected bad column slice.

Regarding Claim 2, Bhavsar discloses an electronic circuit 201 embedded in a RAM circuit chip 12 in an integrated circuit.

Regarding Claim 3, Bhavsar discloses a control circuit (RAM Test Algorithm Engine 207) and address selection circuit (Address and Read/Write Data path Logic 255), which are embedded in a control and address block of the RAM circuit chip 12.

Regarding Claim 4, Bhavsar discloses a BBE 203 part of the control circuit (201), which initiates (begins) testing sequence at power up when the DoPwrBB signal 241 is asserted, or during manufacturing testing when the DoMfgBB signal 242 is asserted. The BBE asserts the Bbedone signal 243 when the test is terminated (completed) and provides a pass/fail signal 244 to indicate whether RAM is repairable. The address selection circuit (255) informs the control circuit (207) when the indexed memory

address (94) equals an initial self-test memory address, and when (94) equals a final self-test memory address.

Regarding Claim 5, Bhavsar discloses an address selection circuit (Address and Read/Write Data path Logic 255) comprising:

Address multiplexers (95 and 96), having address-multiplexer inputs and address-multiplexer outputs, for selecting a particular row and column using the row address portion 94A and the column address 94B portion of the address 94 for RAM array 81. The address multiplexer receives test memory address from (RAM Test Algorithm Engine 207) during the self-test and it also receives normal operational data addresses from core logic 16 which accesses the RAM 80 via the memory bus 20 which carries address, data and control signals.

A row and column repair register 304 and 302 respectively for addressing the RAM 80 memory in writing and reading self-test data.

A sequencer counter 330 and a comparator (XOR 98), which compares the output value 97 with the expected value D0-D82. If the output value 97 is not the same as the expected written value D0 -D82, then the XOR gate outputs a logic "1" to the column ID encoder circuit 100, which provides an error signal 223 and the address 225 of a detected bad column slice.

Regarding Claim 6, Bhavsar discloses an address multiplexer (95 and 96), register (304 and 302), sequencer (counter 330) and comparator (XOR 98), which are all embedded in a control and address block of the RAM circuit chip 12, FIG. 1.

Regarding Claim 8, Bhavsar discloses an input to the error detection circuit (column ID encoder circuit 100) connected to the exclusive-OR-gate (XOR 98) output, FIG. 4.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bhavsar et al. (US 6408401) in view of Gupta et al. (US 6609222).

Regarding Claim 7, Bhavsar substantially discloses a bi-directional memory bus (20, FIG. 1) for writing and reading test or normal data into each slice array (91). Further, he discloses comparator (XOR 98), which compares the output data value (97) from the slice array with the expected data value (D0-D82). However, Bhavsar does not explicitly disclose the exact data-in multiplexing configuration for receiving self-test data or normal operational data for writing into the slice array and an output-complement multiplexer for comparing the test data to data in the slice array.

Furthermore, Gupta in an analogous art discloses FIG. 3 a CAM circuit capable of operating BIST operations including a number of multiplexers (322, 324, and 326) for operating in the BIST mode or in the functional mode. Multiplexer 322 and 324 are

coupled to the row and block address decoders, and the multiplexer 326 is coupled to the read/write port for introducing data to the CAM core during a writing operation. Multiplexer 320 accept search data (e.g., 64 bits of data and 4 tag bits) from a BIST search interface (SIF) 312 and functional search data, and can be controlled to operate in either functional mode or BIST mode.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate the multiplexers, as taught by Gupta, in the bi-directional memory data bus of Bhavsar for the purpose of reading / writing data in a memory device and then comparing the output data from the memory device with a reference data, using a significantly simpler built-in self-test/built-in self-repair (BiST/BiSR) logic. The combined scheme of Bhavsar and Gupta affords a greater flexibility in spare resource allocation and therefore can result in higher yield while utilizing simplified self-test/self-repair logic. A further advantage is the ability of the BIST testing to execute uninterrupted searches at each cycle, while simultaneously performing writes that set up subsequent searches, which enables BIST testing of a CAM core at more realistic speeds.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 22 April 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100